WHAT IS CLAIMED IS:

1. For use in a base station (BS) of a fixed wireless network capable of communicating with a plurality of subscriber transceivers via time division duplex (TDD) channels, a BS transceiver comprising:

a receiver front-end capable of receiving data burst transmissions from said plurality of subscriber transceivers in an uplink portion of a TDD channel, wherein said receiver front-end demodulates said received data burst transmissions into a digital baseband signal in-phase (I) signal and a digital baseband quadrature (Q) signal;

a first frequency domain feedforward equalization filter capable of receiving said I signal and performing a Fast Fourier Transform on a block of N symbols in said I signal to produce a first symbol estimate sequence;

a second frequency domain feedforward equalization filter capable of receiving said Q signal and performing a Fast Fourier Transform on a block of N symbols in said Q signal to produce a second symbol estimate sequence;

an adder capable of receiving said first signal estimate sequence on a first input and said second signal estimate sequence on a second input and producing a combined symbol estimate sequence;

a slicer capable of receiving and quantizing said combined symbol estimate sequence to produce a sequence of decided symbols; and

a time domain feedback filter capable of receiving said sequence of decided symbols and generating a symbol correction sequence that is applied to a third input of said adder.

2. The BS transceiver as set forth in Claim 1 wherein said first frequency domain feedforward equalization filter is 2/T fractionally spaced, where T is a period of said block of said N symbols.

3. The BS transceiver as set forth in Claim 2 wherein said second frequency domain feedforward equalization filter is 2/T fractionally spaced, where T is a period of said block of said N symbols.

4. The BS transceiver as set forth in Claim 1 wherein said time domain feedback filter comprises a delay line comprising D delay taps.

5. The BS transceiver as set forth in Claim 4 wherein said time domain feedback filter uses C feedback coefficients to generate said symbol correction sequence, where C is less than D.

6. The BS transceiver as set forth in Claim 5 wherein said feedback filter is a RAKE filter.

7. The BS transceiver as set forth in Claim 1 further comprising a channel estimation circuit capable of detecting a preamble sequence of symbols in at least one of said I and Q signals and producing therefrom a first plurality of feedforward coefficients usable by said first frequency domain feedforward equalization filter.

8. The receiver as set forth in Claim 7 wherein said channel estimation circuit produces a second plurality of feedforward coefficients usable by said first frequency domain feedforward equalization filter.

9. The receiver as set forth in Claim 1 wherein N=16.

10. A fixed wireless network comprising:

a plurality of base stations capable of communicating with a plurality of subscriber transceivers via time division duplex (TDD) channels, each said base station having a base station (BS) transceiver comprising:

a receiver front-end capable of receiving data burst transmissions from said plurality of subscriber transceivers in an uplink portion of a TDD channel, wherein said receiver front-end demodulates said received data burst transmissions into a digital baseband signal in-phase (I) signal and a digital baseband quadrature (Q) signal;

a first frequency domain feedforward equalization filter capable of receiving said I signal and performing a Fast Fourier Transform on a block of N symbols in said I signal to produce a first symbol estimate sequence;

a second frequency domain feedforward equalization filter capable of receiving said Q signal and performing a Fast Fourier Transform on a block of N symbols in said Q signal to produce a second symbol estimate sequence;

an adder capable of receiving said first signal estimate sequence on a first input and said second signal estimate sequence on a second input and producing a combined symbol estimate sequence;

a slicer capable of receiving and quantizing said combined symbol estimate sequence to produce a sequence of decided symbols; and

a time domain feedback filter capable of receiving said sequence of decided symbols and generating a symbol correction sequence that is applied to a third input of said adder.

11. The fixed wireless network as set forth in Claim 10 wherein said first frequency domain feedforward equalization filter is 2/T fractionally spaced, where T is a period of said block of said N symbols.

12. The fixed wireless network as set forth in Claim 11 wherein said second frequency domain feedforward equalization filter is 2/T fractionally spaced, where T is a period of said block of said N symbols.

13. The fixed wireless network as set forth in Claim 10 wherein said time domain feedback filter comprises a delay line comprising D delay taps.

14. The fixed wireless network as set forth in Claim 13 wherein said time domain feedback filter uses C feedback coefficients to generate said symbol correction sequence, where C is less than D.

15. The fixed wireless network as set forth in Claim 14 wherein said feedback filter is a RAKE filter.

16. The fixed wireless network as set forth in Claim 10 further comprising a channel estimation circuit capable of detecting a preamble sequence of symbols in at least one of said I and Q signals and producing therefrom a first plurality of feedforward coefficients usable by said first frequency domain feedforward equalization filter.

17. The fixed wireless network as set forth in Claim 16 wherein said channel estimation circuit produces a second plurality of feedforward coefficients usable by said first frequency domain feedforward equalization filter.

18. The fixed wireless network as set forth in Claim 10 wherein N=16.